REMARKS

(1) Claims 1-13 and 22-33 are pending in the present application. Claim 1 has been broadened in light of the cited references. Although claims 8 and 9 have been amended, claims 8 and 9 have not been narrowed or broadened by these amendments.

(2) The Office Action cited the following references:

A. U.S. Patent 6,313,024, by Cave et al., entitled *Method for Forming a Semiconductor Device* (referred to as "Cave" hereinafter);

B. U.S. Patent 6,261,944, by Mehta et al., entitled *Method for Forming a Semiconductor Device having High Reliability Passivation Overlying a Multi-Level Interconnect* (referred to as "Mehta" hereinafter);

C. U.S. Patent 6,022,809, by Fan, entitled *Composite Shadow Ring for an Etch Chamber and Method of Using* (referred to as "Fan" hereinafter); and

D. U.S. Patent 5,075,965, by Carey et al., entitled *Low Temperature Controlled Collapse Chip Attach Process* (referred to as "Carey" hereinafter).

(3) **Claim 10** has been rejected under 35 U.S.C. § 102(b) as assertedly being anticipated by Cave. Applicant respectfully traverses this rejection for the following reason.

Cave does not disclose, teach, suggest, or motivate "forming an oxide buffer layer over and abutting the silicon nitride passivation layer, the oxide buffer layer having a thickness substantially smaller than a thickness of the passivation layer," as claim 10 requires. Because Cave does not disclose this aspect required by claim 10, Cave cannot anticipate the invention of claim 10. Thus, Applicant respectfully asserts that claim 10 is patentable over Cave.

(4) Claims 12-13 and 22-26 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave. Claims 1, 6-9 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave in view of Mehta. Claims 2-5, 11, and 29-33 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave in view of Mehta and Fan. Claim

27 was rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave in view of Carey. Applicant respectfully traverses these rejections for the following reasons.

Claims 1-9

The cited references do not disclose, teach, suggest, or motivate a "method of forming post passivation interconnects for an integrated circuit having a plurality of contact regions," where the method includes "removing a top portion of the buffer layer," "depositing a post passivation metal layer over the buffer layer after removing a top portion of the buffer layer," and "forming a connection pattern in the post passivation metal layer such that portions of the connection pattern are electrically coupled to the contact regions," as claim 1 requires.

More specifically, the Office Action states that "Cave fails to disclose expressly the step of removing a top portion of the buffer layer." The Office Action relies on Mehta for teaching this limitation. However, the cited references do not disclose, teach, suggest, or motivate "removing a top portion of the buffer layer" and "depositing a post passivation metal layer over the buffer layer *after* removing a top portion of the buffer layer."

Furthermore, the cited references are not even applicable or relevant because they are not relating to "forming post passivation interconnects for an integrated circuit having a plurality of contact regions." As the background of the patent application states at paragraph [0004]: "In a post passivation interconnect ("PPI") process, contact pads and other conductors are fabricated on top of the passivation layer 18 and connected to the contact regions 16 of the integrated circuit 10. These interconnects can be used to re-route the connections to integrated circuit 10 to facilitate contact to the package."

Some of the advantages of a PPI method are clearly stated in the patent application, and are not mentioned nor taught in the non-PPI references cited. For example, the patent application states at paragraph [0025], "the buffer layer helps to reduce contamination during a subsequent PPI process." This is further discussed in paragraphs [0038], [0046], and [0047]:

> Referring now to FIG. 6c, an optional cleaning of the integrated circuit 10 is cleaned. During this process, an uppermost portion of buffer layer 100 is

> etched. This process is often performed in a cleaning chamber that includes inner wall made primarily from quartz. . . .
>
> These improvements can be possibly explained in a number of ways. With a PPI process that does not include a buffer layer 100, passivation layer 18 is etched before the deposition of post passivation metal layer 20 and/or during etching of metal layer 20 and clusters of silicon nitride are knocked off from the surface of passivation layer 18. These clusters of silicon nitride form particles that do not stick very well to the quartz surface of the cleaning chamber. These particles can contaminate the surface of those integrated circuits that are processed in this chamber. If passivation layer 18 of an integrated circuit is contaminated with these particles, layers of materials on top of passivation layer 18 can peel off and cause defects on the integrated circuit.
>
> Using the improved PPI process in FIGS. 6a-6d, when buffer layer 100 is etched in the cleaning chamber using a ion milling technique before the deposition of post passivation metal layer 20 and/or during etching of metal layer 20, clusters of silicon oxide are knocked off from the surface of buffer layer 100. These clusters of silicon oxide form particles that adhere to the quartz surface on the processing chamber. Thus, the number of particles that can contaminate the surface of integrated circuits being processed is reduced.

These unexpected benefits of reducing the number of defects generated were verified through experimentation, as are illustrated in FIG. 7 of the patent application and discussed at paragraph [0045].

Yet another advantage of a PPI method, which is not mentioned nor taught in the non-PPI references cited, is discussed at paragraph [0030] of the patent application:

> One advantage of using the PPI process is that the configuration of contact regions on integrated circuit 10 can be modified to match the packaging technology. For example, FIG. 5a shows a plan view of the integrated circuit 10 including contact regions 26, conductors 40 and contact regions 16. In this case, the substantially completed integrated circuit included contact regions 16 located around the periphery of the integrated circuit 10. This configuration is convenient for wire bonded packaging processes.

Because none of the references teach the claimed invention of claim 1, combinations of these references cannot teach the claimed invention. Accordingly, Applicant respectfully asserts that independent claim 1 is patentable over the cited references.

Because claims 2-9 depend from claim 1, Applicant respectfully submits that claims 2-9 are patentable over the cited references because of their dependency from independent claim 1 for the reasons discussed above.

Claims 11-13

Claims 11-13 depend from independent claim 10 and add further limitations. As discussed above, claim 10 is allowable and, therefore, the claims that depend from claim 10 are allowable.

Claims 22-28

The cited references do not disclose, teach, suggest, or motivate a "forming an oxide buffer layer overlying the nitride passivation layer, the oxide buffer layer having a thickness substantially smaller than a thickness of the nitride passivation layer" and "forming a post passivation metal layer overlying the oxide buffer layer, the post passivation metal layer patterned so as to electrically couple the plurality of contact regions to a plurality of contact pads formed in the post passivation metal layer," as claim 22 requires.

The cited references are not applicable or relevant because they are not relating to post passivation interconnect processing. As the background of the patent application states at paragraph [0004]: "In a post passivation interconnect ("PPI") process, contact pads and other conductors are fabricated on top of the passivation layer 18 and connected to the contact regions 16 of the integrated circuit 10. These interconnects can be used to re-route the connections to integrated circuit 10 to facilitate contact to the package."

Some of the unexpected advantages of this PPI method are clearly stated in the patent application, which are not mentioned nor taught in the non-PPI references cited. For example, the patent application states at paragraph [0025], "the buffer layer helps to reduce contamination during a subsequent PPI process." Other unexpected advantages are further discussed in paragraphs [0038], [0046], and [0047] (as quoted above). The unexpected benefits of reducing the number of defects generated during processing were verified through experimentation, as are illustrated in FIG. 7 of the patent application and discussed at paragraph [0045].

Because none of the references teach the claimed invention of claim 22, combinations of these references cannot teach the claimed invention. Accordingly, Applicant respectfully asserts that independent claim 22 is patentable over the cited references.

Because claims 23-28 depend from claim 22, Applicant respectfully submits that claims 23-28 are patentable over the cited references because of their dependency from independent claim 22 for the reasons discussed above.

Claims 29-33

Claims 30-33 depend from independent claim 29. Applicant respectfully asserts that Claims 29 is patentable over the cited references for at least the same reasons asserted above regarding claims 1, 10, and 22. Because none of the references teach the claimed invention of claim 29, combinations of these references cannot teach the claimed invention. Accordingly, Applicant respectfully asserts that independent claim 29 is patentable over the cited references.

Because claims 30-33 depend from claim 29, Applicant respectfully submits that claims 30-33 are patentable over the cited references because of their dependency from independent claim 29 for the reasons discussed above.

(5) In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney (contact information provided below). In the event that there are any additional fees due to keep this case pending, please charge such fees, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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